WE CLAIM:

1. A semiconductor device comprising:

a transistor having a source and a drain comprising a substrate material and having a gate trench between the source and the drain; and

an isolation trench filled with a nonconductive material surrounding the transistor,

wherein the gate trench has sidewalls comprising the nonconductive material, which are substantially free of the substrate material.

2. The device of Claim 1, wherein the substrate material comprises silicon.

3. The device of Claim 1, wherein the gate trench has a depth within the range of about 50 nm to about 300 nm.

4. The device of Claim 1, wherein the gate trench has a rounded bottom.

5. The device of Claim 1, wherein the isolation trench has a depth within the range of about 300 nm to about 500 nm.

6. The device of Claim 1, wherein the nonconductive material comprises an oxide material.

7. The device of Claim 1, further comprising a ridge of substrate material between the transistor and the isolation trench, wherein the transistor is separated from the ridge of substrate material by a separation trench filled with the nonconductive material.

8. The device of Claim 7, wherein the separation trench completely surrounds the source and the drain such that the source and the drain do not contact the ridge of substrate material.

9. The device of Claim 7, wherein the separation trench is configured such that one side of the source and one side of the drain are in contact with the ridge of substrate material.

10. An integrated circuit transistor comprising:

a source;

a drain; and

a gate trench between the source and the drain, the gate trench having nonconductive sidewalls and having a first depth,

wherein the transistor is surrounded by an isolation trench having a second depth that is greater than the first depth, and

wherein the nonconductive sidewalls of the gate trench are formed at a point toward the middle of the gate trench and away from the isolation trench.

11. The transistor of Claim 10, wherein the first depth falls within the range of about 50 nm to about 300 nm.

12. The transistor of Claim 10, wherein the gate trench has a rounded bottom.

13. The transistor of Claim 10, wherein the second depth falls within the range of about 300 nm to about 500 nm.

14. The transistor of Claim 10, further comprising a ridge of substrate material between the transistor and the isolation trench, wherein the transistor is separated from the ridge of substrate material by a separation trench.

15. The transistor of Claim 14, wherein the separation trench completely surrounds the source and the drain such that the source and the drain do not contact the ridge of substrate material.

16. The transistor of Claim 14, wherein the separation trench is configured such that one side of the source and one side of the drain are in contact with the ridge of substrate material.

17. A method of forming a semiconductor element comprising:

providing a semiconductor substrate having a hard mask layer deposited thereon;

patterning the hard mask layer with a first photo mask;

etching the semiconductor substrate to form an isolation trench having a first depth;

patterning the hard mask layer with a second photo mask; and

etching the semiconductor substrate to form a gate trench having a second depth and simultaneously etching the isolation trench to a third depth, wherein the third depth is greater than the second depth.

18. The method of Claim 17, wherein the hard mask layer comprises TEOS, amorphous carbon, silicon nitride, silicon oxynitride, or silicon carbide.

19. The method of Claim 17, wherein the hard mask layer has a thickness within the range of about 100 Å to about 700 Å.

20. The method of Claim 17, wherein etching the semiconductor substrate to form an isolation trench comprises ion milling, reactive ion etching, or chemical etching.

21. The method of Claim 20, wherein etching the semiconductor substrate to form an isolation trench comprises using Cl_2 as an etchant.

22. The method of Claim 17, wherein the second photo mask comprises at least one feature that is sized to allow for possible mask misalignment.

23. The method of Claim 17, wherein etching the semiconductor substrate to form a gate trench comprises ion milling, reactive ion etching, or chemical etching.

24. The method of Claim 23, wherein etching the semiconductor substrate to form a gate trench comprises using Cl_2 as an etchant.

25. The method of Claim 17, further comprising:

filling the gate trench and the isolation trench with a nonconductive material;

patterning the nonconductive material with a third photo mask; and

etching the nonconductive material out of a region of the gate trench to form a trench having nonconductive sidewalls.

26. The method of Claim 25, wherein filling the gate trench and the isolation trench with a nonconductive material comprises performing CVD or PVD.

27. The method of Claim 25, further comprising polishing the nonconductive material to expose an underlying source and drain.

28. The method of Claim 27, wherein polishing the nonconductive material comprises performing CMP.

29. The method of Claim 25, wherein the third photo mask comprises at least one feature that is sized to allow for possible mask misalignment.

30. The method of Claim 25, wherein etching the nonconductive material comprises ion milling, reactive ion etching, or chemical etching.

31. The method of Claim 30, wherein etching the nonconductive material comprises using CF_4 as an etchant.

32. A method of fabricating a transistor comprising;

patterning a substrate with a first mask;

forming an isolation trench in the substrate;

depositing a nonconductive material in the isolation trench;

patterning the substrate with a second mask;

forming a gate trench surrounded by a ridge of substrate material, wherein the ridge of substrate material is separated from a source, a drain and a gate by a separation trench;

filling the gate trench and the separation trench with the nonconductive material;

patterning the nonconductive material with a third mask; and

removing the nonconductive material from a region of the gate trench, thereby forming a trench with sidewalls comprising the nonconductive material.

33. The method of Claim 32, wherein the second mask extends into the area in which the isolation trench is formed.

34. The method of Claim 32, wherein the third mask contains at least one feature that is sized to allow for possible mask misalignment.